

REMARKS

Applicants have amended claim 3 to replace the term “supporting substrate” with the more general term “supporting member.” Applicants have added new claims 17 and 18, which find support, for example, at page 5, lines 7-21, and page 8, lines 1-8, of the specification.

Claims 1-16 are pending in this application. Applicants agree with the Examiner that claims 5, 8 and 9 depend from claim 1, and not from claim 3, and thus belong to the nonelected species.

Applicants thank the Examiner for indicating allowable subject matter.

The Examiner requested that the Title be indicative of the claimed invention. Applicants have amended the Title accordingly.

Claim 3 has been rejected under 35 USC 102(b) as anticipated by U.S. Patent Application Publication No. 2002/0013061 (Siniaguine). Applicants respectfully traverse this rejection.

Claim 3 recites bonding a supporting substrate to a first surface of a semiconductor wafer on which a semiconductor element is formed, forming a groove in the semiconductor wafer by etching a second surface of the semiconductor wafer, which is opposite to the first surface, and rounding a corner of the groove by etching the second surface. The Examiner contends that the etching steps shown in FIGS. 9-11 of Siniaguine correspond to the claimed manufacturing method and equates Siniaguine’s layer 310 to the claimed supporting substrate. Even though the Examiner does not refer to any portion of Siniaguine for the teachings of the claimed semiconductor wafer and the groove, applicants assume, from Siniaguine’s explanation of the drawings, that the Examiner meant to equate Siniaguine’s semiconductor wafer 210 to the claimed semiconductor wafer and Siniaguine’s grooves 260 to the claimed grooves. Applicants respectfully disagree.

As recited above, claim 3 states that the groove is formed in the semiconductor wafer by etching the second surface of the semiconductor wafer which is opposite to the first surface of the semiconductor wafer on which the element is formed and to which the supporting substrate is bonded. In other words, in the claimed manufacturing method, the surface of the wafer in which

the groove is formed is different from the surface of the wafer to which the supporting substrate is bonded. In the meantime, in Siniaguine's method, device elements are formed on the wafer top surface 210F as explained at paragraph [0021], grooves 260 are also formed in the wafer top surface 210F as explained at paragraph [0023], and then layer 310 is formed over grooves 260 on the same wafer top surface 210F as explained at paragraph [0035]. Accordingly, Siniaguine's method does not form the grooves in the wafer surface opposite to the wafer surface to which the supporting substrate is bonded as claimed. Applicants note that Siniaguine does disclose etching from wafer backside surface 110B. However, this etching from the backside is "a blanket (unmasked) uniform etch of the wafer's flat semiconductor backside surface," and not the claimed backside etching to form a groove. See paragraph [0027] of Siniaguine.

The rejection of claim 3 under 35 USC 102(b) on Siniaguine should be withdrawn because Siniaguine does not teach or suggest the claimed etching to form a groove in the second surface of the wafer opposite to the first surface of the wafer to which the supporting substrate is bonded.

In light of the above, a Notice of Allowance is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorize the Commissioner to charge

the cost of such petitions and/or other fees due in connection with the filing of this document to
Deposit Account No. 03-1952, referencing Docket No. **606402016900**.

Respectfully submitted,

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